13
5-7-03
Mobil

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

GLEN WADA
R. V. GIRIDHAR
ANTHONY OZZELLO

Serial No.: 10/052,853

Filed: November 9, 2001

For: FLASH MEMORY WITH UV OPAQUE PASSIVATION LAYER

Art Unit: 2813

Examiner: J. Chen

Attorney Docket: 042390.P7196D

Assistant Commissioner for Patents and Trademarks
Washington, D.C. 20231

APPEAL BRIEF UNDER 37 C.F.R. §1.192

Dear Sir:

Applicants hereby submit this brief in support of their appeal from a final decision of the examiner in the captioned case. The filing deadline is May 4, 2003 -- the last day of the two month filing period following the Patent Office's March 4, 2003 receipt of applicants' notice of appeal.

(1) REAL PARTY IN INTEREST

Intel Corporation of Santa Clara, CA.

(2) RELATED APPEALS AND INTERFERENCES

None.

(3) STATUS OF CLAIMS

In this application, claims 9-15 are pending. Claims 9-15 stand rejected under 35 U.S.C. § 112, first paragraph. Claims 9-11 and 15 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kiyohiko (JPO Publication Number 04-078,173). Claims 12-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kiyohiko (JPO Publication Number 04-078,173) in view of Jeuch (U.S. Patent Number 5,138,573).

The applicants appeal the rejection of claims 9-15 for failure to comply with 35 U.S.C. § 112, first paragraph; the rejection of claims 9-11 and 15 under 35 U.S.C. § 102(b) as being anticipated by Kiyohiko; and the rejection of claims 12-14 under 35 U.S.C. § 103(a) as being unpatentable over Kiyohiko in view of Jeuch.

(4) STATUS OF AMENDMENTS

A final office action was mailed November 25, 2002 rejecting claims 9-15 for the reasons specified above. Those claims were not amended subsequent to final rejection.

The appendix of this brief reflects the claims as applicants understand them to stand as of the date of this appeal.

(5) SUMMARY OF THE INVENTION

The invention relates to flash memories -- a special class of electrically programmable read only memory. Flash memories may be erased and reprogrammed electronically. They differ from other types of electrically programmable read only memories ("EPROMs)", e.g., those which can be erased only by exposing their memory cells to ultraviolet ("UV") light. With the advisory action, the examiner enclosed a textbook excerpt that describes flash memories as a form of EEPROM. The term "EPROM" thus refers to different classes of devices: (1) flash memories, which may be erased electronically, (2) other kinds of electronically erasable programmable read only memories, and (3) electrically programmable read only memories that can be erased only by exposing them to UV light. The term EPROM and the term flash memory are not synonymous, as flash memories are a subset of a broader category of devices known generically as EPROMs.

Processes for making flash memories cause charge to build up on the floating gates of the flash memory cells. That charge must be neutralized. Prior to applicants' invention, processes for making flash memories neutralized charge by exposing the devices to UV light at the end of the process. Because the UV exposure step took place after the passivation layer was formed, only UV transparent materials could be used to make the passivation layer. The specification, at page 2, lines 9-25, describes the prior art process for making flash memories.

Applicants discovered that a UV exposure step could effectively neutralize electric charge – even when applied before the passivation layer was formed, as long as that UV exposure step was performed after the final metal layer was patterned. Applicants' process for making a flash memory, which includes applying a UV exposure step before forming the passivation layer, is the subject of U.S. Patent No. 6,350,651.

Because the standard process for making flash memories exposed the passivation layer to UV light after it was formed, the flash memories that preceded applicants' invention had to include a passivation layer that was transparent to UV light. Applicants' patented method, which applies the UV exposure step before the passivation layer is formed, enabled -- for the first time – a flash memory with a UV opaque passivation layer.

Applicants' figure 1, as described in the specification at page 5, lines 1-6, illustrates such a flash memory. That flash memory includes UV opaque passivation layer 103. Figure 1 shows that passivation layer 103 covers semiconductor substrate 101. The specification, at page 3, lines 20-22, specifies that the semiconductor substrate 101 "includes conventional flash memory features, including flash memory cells (not shown)." Because the drawings show passivation layer 103 covering substrate 101, which includes flash memory cells, it must follow that figure 1 illustrates passivation layer 103 covering the flash memory cells. Applicants' claim 9 specifies that the flash memory includes a flash memory cell and a passivation layer "that is not transparent to ultraviolet light, the passivation layer covering the flash memory cell."

(6) ISSUES

In the final office action mailed November 25, 2002, the examiner rejected claims 9-15 under 35 U.S.C. § 112, first paragraph, claims 9-11 and 15 under 35 U.S.C. § 102(b) as being anticipated by Kiyohiko, and claims 12-14 under 35 U.S.C. § 103(a) as being unpatentable over Kiyohiko in view of Jeuch.

The questions presented on this appeal are:

(1) Whether the specification contains a written description of the invention, as 35 U.S.C. § 112, first paragraph, requires.

(2) Whether Kiyohiko anticipates the invention of claims 9-11 and 15 under 35 U.S.C. § 102(b).

(3) Whether the combination of Kiyohiko and Jeuch would have rendered the invention of claims 12-14 obvious under 35 U.S.C. § 103(a).

(7) GROUPING OF CLAIMS

For question (1), claims 9-15 are grouped together.

For question (2), claims 9-11 and 15 are grouped together.

For question (3), claims 12-14 are grouped together.

(8) ARGUMENT

Question 1 -- Whether the specification contains a written description of the invention, as 35 U.S.C. § 112, first paragraph, requires.

In the final office action, the examiner rejected claims 9-15 under 35 U.S.C. § 112, first paragraph, because the phrase "the passivation layer covering the flash memory cell," which appears in claim 9 (the only independent claim), purportedly is not supported by the original disclosure. As explained in detail below, that rejection is in error because the specification and drawings adequately support that phrase – even though the specification does not use the exact language that appears in claim 9.

To comply with the written description requirement, the specification need not describe the claimed subject matter in exactly the same terms as used in the claims; it must simply indicate to persons skilled in the art that as of the filing date the applicant had invented what is now claimed. The failure of the specification to specifically mention a limitation that later appears in the claims is not a fatal one when one skilled in the art would recognize upon reading the specification that the new language reflects what the specification shows has been invented. All Dental Prodx, LLC v. Advantage Dental Prods, Inc., 309 F.3d 774 (Fed. Cir. 2002). If a person of ordinary skill in the art would have understood the inventor to have been in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification, then the adequate written description requirement is met. In re Alton, 76 F.3d 1168, 1175 (Fed. Cir. 1996).

One skilled in the art would recognize -- upon reading applicants' specification in conjunction with applicants' drawings -- that the phrase "the passivation layer covering the flash memory cell" (added to original claim 9) reflects what applicants' specification and drawings show applicants invented. Applicants' figure 1 shows passivation layer 103 covering semiconductor substrate 101. The specification states, at page 3, lines 20-22, that semiconductor substrate 101 "includes conventional flash memory features, including flash memory cells (not shown)." Because passivation layer 103 covers substrate 101, which includes flash memory cells, it necessarily follows that passivation layer 103 covers the flash memory cells.

The specification (at page 6, line 3, through page 7, line 2) further demonstrates that passivation layer 103 must cover the claimed flash memory's flash memory cells. Here, the specification describes forming a UV opaque passivation layer, which comprises a silicon nitride barrier layer 104 and a polyimide stress reduction layer 105. The silicon nitride layer is formed using a conventional plasma enhanced chemical vapor deposition ("PECVD") process, and the polyimide layer is "spun onto the silicon nitride layer." Because such PECVD and spin-on processes deposit materials over the entire structure, the resulting passivation layer must necessarily cover the device's flash memory cells. As the specification indicates at page 5, lines 5 and 6, part of passivation layer 103 is subsequently removed to define bond pads – not to expose the underlying flash memory cells.

For these reasons alone, anyone skilled in the art will immediately recognize that the structure applicants described in the original specification includes a passivation layer that covers the claimed device's flash memory cells. This is even more evident given that the essence of applicants' patented process is that it permits a UV opaque passivation layer to cover the flash memory cells of a flash memory. As explained in the Background of the Invention section of the specification (page 2, lines 9-25), charge may build up on the floating gates of the flash memory cells as the device is made. Prior to applicants' invention, the device was exposed to UV radiation to neutralize that charge after the passivation layer was formed. As a result, previous flash memories could not include a UV opaque passivation layer because such a layer would prevent UV radiation from reaching the flash memory cells' floating gates. A UV opaque passivation layer would prevent UV radiation from reaching the flash memory cells because the passivation layer covered them.

To enable a flash memory to include a UV opaque passivation layer, applicants devised the process claimed in U.S. Patent No. 6,350,651. That patent issued from the parent application from which this pending divisional application claims priority. That process exposes the device to UV light to neutralize process induced charge before forming the passivation layer. This change in process sequence enables a UV opaque passivation layer to be formed – notwithstanding the fact that the passivation layer must cover the flash memory cells. There would not be any advantage to applicants' new process,

over prior practice, unless the passivation layer in the claimed flash memory covered the flash memory cells.

Because the passivation layer in a flash memory device covers the flash memory cells, prior processes required a UV transparent passivation layer to enable UV light to reach the flash memory cells. Applicants' patented process enables a UV opaque passivation layer to be used instead -- despite the fact that it covers the flash memory cells, because applicants' process exposes the device to UV light (to neutralize process induced charge) before forming the passivation layer. Anyone skilled in the art would thus appreciate, based on the basic structure of flash memories and the nature of applicants' patented process, that applicants' specification must disclose a flash memory with a passivation layer that covers the flash memory cells.

For the reasons set forth above, applicants' specification adequately supports the phrase "the passivation layer covering the flash memory cell," despite not including these precise words. In re Wright, 866 F.2d 422 (Fed. Cir. 1989), compels this finding. In that case, the Court of Appeals for the Federal Circuit reversed a decision from the Board of Patent Appeals and Interferences, which had upheld the rejection of an amended claim under 35 U.S.C. §112, first paragraph, based on the specification supposedly not providing an adequate written description of a particular element.

In In re Wright, the rejected claim covered a method of forming images that included depositing a layer of photosensitive microcapsules in the form of a free-flowing powder. The claim had been amended by adding a limitation, which

specified that the powder be "distributed upon said support but not permanently fixed thereto." The specification, as filed, did not include the exact phrase "not permanently fixed." Nonetheless, the Court held that the original disclosure unequivocally taught the absence of permanently fixed microcapsules. The Court supported that conclusion by noting that the specification's examples indicated that the microcapsules should be distributed so as not to change their position until the image is formed. Because those examples suggested that the microcapsules' position would be changed after the image was formed, they demonstrated that the microcapsules were not permanently fixed – as specified in the amended claim.

As in In re Wright, applicants' drawings and specification indicate that the passivation layer must cover the flash memory cells – even though the specification does not provide the precise language that was added to amended claim 9. That disclosure -- which describes applying the UV exposure step before forming the passivation layer, thereby, enabling a UV opaque passivation layer to cover the flash memory cells -- adequately supports the phrase "the passivation layer covering the flash memory cell." Accordingly, applicants respectfully request the Board to vacate the examiner's final rejection of claims 9-15 under 35 U.S.C. §112.

Question 2 -- Whether Kiyohiko anticipates the invention of claims 9-11 and 15 under 35 U.S.C. § 102(b).

In the final office action, the examiner rejected claims 9-11 and 15 as purportedly being anticipated by Kiyohiko. That rejection is in error because Kiyohiko does not anticipate the flash memory of claim 9.

Claim 9 defines a flash memory. A flash memory is a type of electrically programmable read only memory that is erased electronically. Kiyohiko does not describe a flash memory, but instead describes an EPROM that is erased by exposing it to UV radiation. The examiner's reliance on page 2, lines 13-14, of applicants' specification -- to support the contention that the terms EPROM and flash memory are synonymous -- is misplaced. That excerpt simply mentions that flash memories are erasable programmable read only memories that may be erased electrically. It does not suggest (nor was it intended to suggest) that a UV erasable EPROM, like the one Kiyohiko describes, is a flash memory. Because Kiyohiko describes a UV erasable EPROM – not a flash memory, that reference does not anticipate claim 9.

Kiyohiko does not anticipate that claim for another reason. Claim 9 requires the UV opaque passivation layer to cover the flash memory cell. Because flash memories do not require UV exposure to erase them, they may remain operable even when their flash memory cells are covered with such a passivation layer. As explained above, applicants' patented process permits a flash memory to include a UV opaque passivation layer, because that process –

unlike previous processes -- applies the required UV exposure step before the passivation layer is formed.

Unlike applicants' claimed flash memory, Kiyohiko's UV erasable EPROM must permit UV radiation to reach its memory cells. For that reason, Kiyohiko's device must include a window within the passivation layer (e.g., its window 11, which is formed within polyimide film 10) to enable UV radiation to reach its memory cells. Because Kiyohiko's EPROM does not (and cannot) include a passivation layer that covers its memory cells, Kiyohiko's device does not anticipate the flash memory of applicants' claim 9 for this additional reason.

The examiner's contention that Kiyohiko's passivation layer covers the "flash memory cells" is without merit. Because Kiyohiko's device is not a flash memory, it lacks flash memory cells that a passivation layer may cover. Moreover, as already noted, Kiyohiko's UV erasable EPROM cannot function if a UV opaque passivation layer covers its memory cells. To erase Kiyohiko's EPROM, UV light must reach the device's memory cells. That is why Kiyohiko cannot retain the passivation layer where it covers the memory cells.

Although silicon nitride film 9 remains above the memory cells after polyimide film 10 is removed, no one skilled in the art would consider a silicon nitride film to be a UV opaque passivation layer, as the examiner claims. Note that Kiyohiko states that the "passivation film is composed of a silicon nitride film 9 . . . and a polyimide film 10." Because only the silicon nitride film 9 remains above the memory cells in Kiyohiko's UV erasable EPROM, Kiyohiko does not

describe a device that includes a UV opaque passivation layer that covers a flash memory cell, as claim 9 requires.

Notwithstanding Kiyohiko's figure 1, which shows that polyimide film 10 does not cover a memory cell, the examiner contends that an excerpt from that reference teaches to maintain a UV opaque passivation film over at least some of the memory cells. Kiyohiko mentions that "It is not necessary to provide the window 11 to each EPROM element." The examiner interprets that statement as indicating that a UV opaque passivation film may cover at least some memory cells. When relying on that excerpt, however, the examiner neglects the remainder of the sentence, which states: "one [i.e., a window] can be provided to an entire of the [sic] EPROM part." Read in context, that sentence simply offers an alternative to forming a discrete window for each EPROM element to enable UV light to access each element – namely, to instead incorporate into the device a window that exposes the entire EPROM part. That sentence does not suggest that Kiyohiko's device may include a UV opaque passivation layer that covers one or more memory cells. On the contrary, it simply indicates that the memory cells may be exposed either by discrete or blanket removal of the passivation layer.

The examiner noted that parts of the UV opaque passivation layers for both Kiyohiko's UV erasable EPROM and applicants' flash memory have been removed. The examiner seems to conclude, based upon this observation, that parts of those passivation layers were removed for the same reason. Such is not the case. Kiyohiko removes part of polyimide film 10 to expose the memory

cells, thereby, enabling UV light to erasure them. Applicants remove part of the passivation layer to enable bond pads to be formed on the device – while retaining the passivation layer where it covers the flash memory cells. Kiyohiko's retention of silicon nitride film 9 shows that polyimide film 10 was not removed to enable bond pad formation. (Compare Kiyohiko's device, which retains silicon nitride film 9, with applicants' device, which removes silicon nitride layer 104 in addition to polyimide layer 105 where bond pads will be formed.) Removing different parts of their respective UV opaque passivation layers for different reasons, when making Kiyohiko's device and when making applicants' device, does not suggest that Kiyohiko's UV erasable EPROM includes a UV opaque passivation layer that covers a flash memory cell.

The claimed invention relates to flash memories, not UV erasable EPROMs. In addition, the claimed invention requires the UV opaque passivation layer to cover the flash memory cell – a feature that Kiyohiko's UV erasable EPROM necessarily lacks. For these reasons, Kiyohiko does not anticipate the flash memory of claim 9. Because claims 10, 11 and 15 depend upon claim 9, Kiyohiko cannot anticipate the flash memory of those dependent claims either. Accordingly, applicants respectfully request the Board to vacate the examiner's rejection of claims 9-11 and 15 based on Kiyohiko purportedly anticipating them.

Question 3 -- Wheth r the combination of Kiyohiko and Jeuch would have rendered the invention of claims 12-14 obvious under 35 U.S.C. § 103(a).

In the final office action, the examiner rejected claims 12-14 as being unpatentable over Kiyohiko in view of Jeuch under 35 U.S.C. § 103(a). That rejection is in error because the combination of Kiyohiko and Jeuch would not have rendered obvious the inventions that these claims define.

Claims 12-14 depend upon claim 9. As explained above, claim 9 requires the UV opaque passivation layer to cover the flash memory cell. Neither Kiyohiko nor Jeuch describes a flash memory that includes this feature. Nor does either reference provide any teaching or suggestion that would have motivated one skilled in the art to modify any of the devices they describe by incorporating into them a UV opaque passivation layer that covers a flash memory cell.

On the contrary, Kiyohiko teaches away from including such a feature in a flash memory. Kiyohiko teaches to form a window through polyimide film 10 to enable UV radiation to reach the memory cells. Kiyohiko's polyimide film requires such a window because the memory cells of Kiyohiko's UV erasable EPROM can be erased only by exposing them to UV radiation. Replacing Kiyohiko's polyimide film, which must include such a window, with an opaque passivation layer that covers the memory cells yields an inoperable device because such a passivation layer prevents UV radiation from reaching the memory cells. Because those skilled in the art would have recognized that covering the memory cells in Kiyohiko's EPROM with a UV opaque passivation

layer would generate a defective device, it would not have been obvious to them to modify that device in that way.

Unlike Kiyohiko's UV erasable EPROM, flash memories do not require UV exposure to erase them. For that reason, they may be erased even when their flash memory cells are covered with a UV opaque passivation layer. Notwithstanding that fact, conventional wisdom – prior to applicants' invention – held that even flash memories could not include a UV opaque passivation layer that covers the flash memory cells. These devices' memory cells required UV exposure to neutralize any electronic charge that had built up on them during the process for making the device. Because that UV exposure step was performed after the passivation layer was formed, it was not possible for the device to include a UV opaque passivation layer that covered the flash memory cells.

Applicants discovered that such a UV exposure step could effectively neutralize electric charge -- even when applied before forming the passivation layer, as long as that UV exposure step was performed after patterning the final metal layer. Not until applicants invented that now patented process was it even possible to make the flash memory of claim 9, which includes a UV opaque passivation layer that covers the flash memory cell. It logically follows that the claimed flash memory is patentable for essentially the same reasons that the process for making it is patentable – as the United States Patent and Trademark Office previously acknowledged when issuing U.S. Patent No. 6,350,651.

Because neither Kiyohiko nor Jeuch provides any teaching that would have motivated one skilled in the art to modify any of the devices they describe

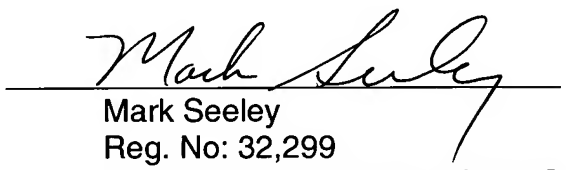
to generate the flash memory of claim 9, that flash memory would not have been obvious in view of their combination. Because claims 12-14 depend upon claim 9, they are likewise patentable over the cited prior art. Accordingly, applicants respectfully request the Board to vacate the examiner's rejection of claims 12-14 under 35 U.S.C. §103(a) based on the combination of Kiyohiko and Jeuch.

CONCLUSION

For the foregoing reasons, the Board is respectfully requested to vacate the examiner's rejections of claims 9-15, to remand this application to the examiner, and to direct the examiner to pass this case to issuance.

Respectfully submitted,

Date: April 24, 2003



Mark Seeley
Reg. No: 32,299
ATTORNEY FOR APPLICANTS

Intel Corporation
Mail Stop SC4-202
2200 Mission College Blvd.
Santa Clara, CA 95052-8119
(408) 765-7382

APPENDIX

Shown below is a copy of the claims involved in the appeal, as the applicants understand them to stand.

9. A flash memory comprising:

a semiconductor substrate that includes a flash memory cell that has a floating gate;

a conductive layer formed on the substrate; and

a passivation layer formed on the conductive layer that is not transparent to ultraviolet light, the passivation layer covering the flash memory cell.

10. The flash memory of claim 9 wherein the passivation layer comprises a barrier layer and a stress reduction layer.

11. The flash memory of claim 10 wherein the passivation layer comprises a silicon nitride layer and a polyimide layer.

12. The flash memory of claim 11 wherein the flash memory cell's floating gate has a gate length that is less than about 0.5 microns.

13. The flash memory of claim 12 wherein the conductive layer forms the final metal interconnect for the flash memory, upon which is formed the passivation layer.

14. The flash memory of claim 13 wherein the silicon nitride layer is between about 2,000 and about 10,000 angstroms thick.

15. The flash memory of claim 9 wherein the passivation layer comprises a polyimide layer.

FIRST CLASS CERTIFICATE OF MAILING
(37 C.F.R. § 1.8(a))

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail with sufficient postage in an envelop addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on

April 24, 2003
Date of Deposit

Mark Seeley
Name of Person Mailing Correspondence

Mark Seeley
Signature

April 24, 2003
Date